Intel StrataFlash® Wireless Memory (L18) to Intel® PXA270 Processor Design Guide

Application Note 777

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Contents

Revision History

Date	Revision	Description
6/04	001	Initial Release
10/04	002	- Changed PXA27x to PXA270 - Added a nRESET_OUT note - Updated Appendix A, Additional Information - Minor text edits

1.0 Introduction

This application note describes interfacing the following devices:

- Intel StrataFlash® Wireless Memory (L18), hereafter in this document referred to as Intel® L18 flash memory
- Intel® PXA270 Processor

It discusses general concepts involved when interfacing to the integrated features and control signals of the L18. It is assumed that you possess a working knowledge of the devices discussed in this document.

This document was written based on information available at the time, specifically the Intel® 28F128L18 flash memory device and Intel® PXA270 processor. Any changes in specifications to either device may not be reflected in this document. Refer to the appropriate documents or sales personnel for the most current information before finalizing any design.

1.1 Intel StrataFlash® Wireless Memory (L18)

Intel StrataFlash® Wireless Memory (L18) combines reliable and proven multi-level cell (MLC) technology with multi-partition read-while-write (RWW) and read-while-erase (RWE) dual operation. Combining high read performance with the flash memory intrinsic non-volatility, Intel® L18 flash memory eliminates the traditional system-performance paradigm of shadowing redundant code memory from slow nonvolatile storage into faster execution memory, thereby reducing the total memory requirement, increasing reliability, and reducing overall system power consumption and cost.

The Intel® L18 flash memory flexible multi-partition architecture allows programming or erasing to occur in one partition while reading from another partition. This allows for higher data-write throughput as compared to a single partition device. This dual-operation architecture enables a processor to perform code-fetch reads while program or erase operations take place in the background. The system designer can also choose the size of the system's code and data partitions via the flexible multi-partition architecture of the Intel® L18 flash memory.

The Intel® L18 flash memory also features high-performance asynchronous page- and synchronous burst-read modes using 1.8 V low-voltage MLC technology. The logic-core voltage of the L18 is 1.8 V (V_{CC}), but there are two I/O voltage (V_{CCQ}) options, -1.8 V (L18) and 3 V (L30). The L18 is manufactured on Intel ETOX™ VIII process technology (0.13 um).

1.2 Intel® PXA270 Processor

The Intel® PXA270 processor family utilizes an integrated system-on-a-chip microprocessor for high performance, low power portable handheld and handset devices. It incorporates the Intel® XScale™ micro architecture with on-the-fly voltage and frequency scaling, and sophisticated power management to provide industry-leading MIPS/mW performance.

Intel XScale is a 32-bit RISC micro architecture that is ARM* architecture compliant. The Intel® PXA270 processor also provides a powerful multimedia coprocessor which supports Intel MMX™ integer instructions to accelerate audio and video processing.

The Intel® PXA270 processor contains a 32-KByte instruction cache and a 32-KByte data cache, using a 256-bit line-fill buffer.

The on-chip memory controller is based on a Unified Memory Architecture wherein all external memory devices share a common address and data bus, and the external memory space is viewed as a linear collection of bytes numbered upwards from 0. The memory controller consists of four main control units for interfacing with synchronous dynamic memory (SDRAM), static memory (SRAM; includes ROM and Flash memory), PCMCIA, and companion chips.

The static memory space supports Intel® flash memory in asynchronous 4- or 8-word page-read modes, and synchronous 8- or 16-word burst-read modes. Bus widths of 16- and 32-bits is also supported, with a maximum addressability of 64 Mbytes per chip select. Bus clock rates are:

- 26 to 104 MHz for SDRAM
- 26 to 65 MHz for synchronous SRAM and burst flash memory

2.0 Hardware Interface

This section describes the hardware interface signals between the Intel® L18 flash memory and the Intel® PXA270 processor. This document assumes that all other device signals and power supplies are connected to ensure proper device operation.

2.1 Intel® Flash Memory Interface

The Intel® L18 flash memory integrates several hardware features that enable it to be used with a range of burst processors such as the Intel® PXA270 processor. These features include:

- Address Latch (ADV#) input signal
- Read Configuration Register (RCR)
- Internal burst-address generator
- Programmable WAIT signal polarity

The address latch (ADV#) is used to latch the address during read operations. CPUs that employ a multiplexed address/data bus can utilize the internal latch to de-multiplex the bus. ASICs can also use the latch to reduce pin count while improving performance.

The Read Configuration Register (RCR) is used to configure the flash memory component to specific CPU characteristics. These include synchronous or asynchronous read mode, burst length (4-, 8-, 16-, or continuous-word), burst latency, valid clock edge and WAIT configuration.

The RCR settings also inform the internal burst-address generator how to generate addresses during synchronous-burst reads. Generating addresses internally eliminates the memory's dependence on the CPU for the next address during a burst read, improving system read performance.

The hardware interface of the Intel® L18 flash memory has the following signals:

A[max:0] ADDRESS: Device address inputs. 64Mbit: A[21:0]; 128Mbit: A[22:0]; 256Mbit: A[23:0]. A0 is a word (x16) address bit.

D[15:0] DATA I/O: Inputs during write operations or outputs during read operations; High-Z (float) when CE# or OE# are deasserted.

CE# CHIP ENABLE: Low-true input; CE#-low enables the device. CE#-high disables the device, placing it in standby mode. CE#-high places data and WAIT signals at High-Z.

OE# OUTPUT ENABLE: Low-true input; OE#-low enables the output buffers. OE#-high disables the output buffers and places all data outputs and WAIT in High-Z.

WE# WRITE ENABLE: Low-true input; WE#-low enables the write buffers. Address and data are latched on the rising edge of WE#.

WP# WRITE PROTECT: Low-true input; WP# enables and disables the lock-down mechanism. WP#-low enables the lock-down mechanism - blocks configured for lock-down cannot be unlocked with software commands. WP#-high overrides the lock-down mechanism enabling software to unlock blocks.

CLK CLOCK: Input; configurable as valid rising edge or valid falling edge. CLK synchronizes the device to the system bus clock and increments the internal address generator in synchronous-burst read mode. In synchronous-burst read mode, the initial address is latched on the rising edge of ADV# or the next valid clock edge when ADV# is low, whichever occurs first.

ADV# ADDRESS VALID: Low-true input. In synchronous-burst read mode, the initial address is latched on the rising edge of ADV# or the next valid clock edge when ADV# is low, whichever occurs first.

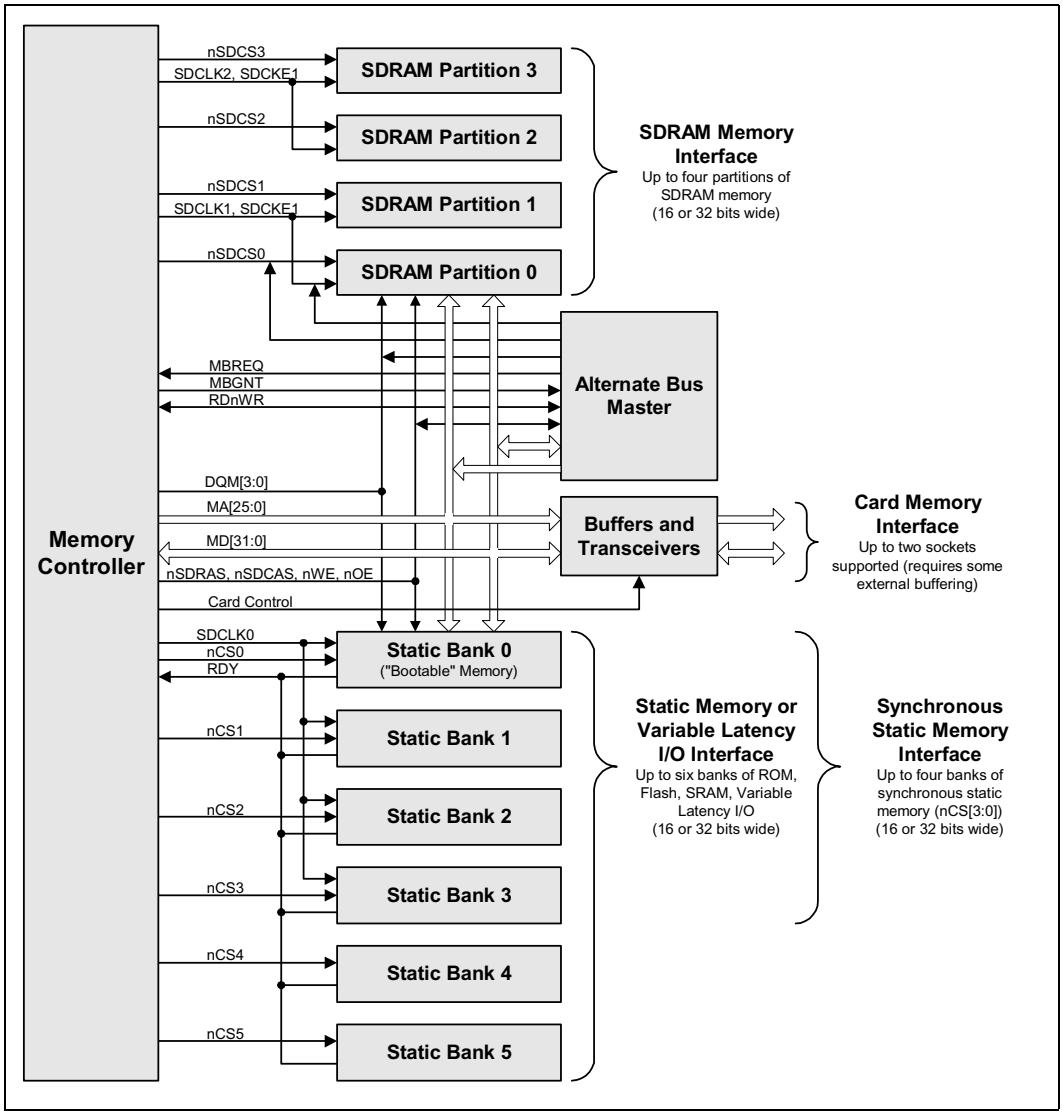
WAIT WAIT: Output; configurable for high-true or low-true. In synchronous-burst read mode, WAIT indicates invalid data when asserted and valid data when deasserted. WAIT is High-Z whenever CE# or OE# is deasserted. WAIT cannot be used with XScale processors, therefore it is not needed by this design example.

RST# RESET: Low-true input. RST# resets internal automation and inhibits write operations. RST#-high enables normal operation.

2.2 Intel® PXA270 Processor External Memory Interface

The external memory interface of the Intel® PXA270 processor supports a variety of memory types. Its external memory bus supports SDRAM, page and burst mode flash memory, synchronous masked ROM (SMROM), page-mode ROM, SRAM, SRAM-like Variable Latency I/O (VLIO) memory, PCMCIA expansion memory, and compact flash (see Figure 1). Memory types are programmable through the Intel® PXA270 processor memory controller configuration registers.

Figure 1. Intel® PXA270 Memory Interface Configuration



The Intel® PXA270 processor uses the following external memory interface signals:

MA[25:0] Memory Address Bus. The memory address bus transfers address information between the processor and external memory.

MD[31:0] Memory Data bus. The memory data bus carries data between the processor and external memory.

SDCLK[2:0]	Rising-edge clock outputs used to synchronize data transfers between the processor and the selected external memory. SDCLK0 is used for Static Banks 0, 1, 2, and 3. SDCLK1 is for SDRAM partitions 0 and 1; SDCLK2 is for SDRAM partitions 2 and 3.
SDCKE1	High-true output; clock enable for all SDRAM partitions.
nSDCAS	SDRAM Column Address Strobe. Low-true, nSDCAS is used to latch the initial-access address during burst reads from synchronous flash memory.
nCS[5:0]	Static Memory Chip Selects. Low-true outputs, the chip selects are individually programmable through the memory configuration registers. All six static memory chip selects support asynchronous page-read mode; however, only nCS[3:0] support synchronous burst-read mode. nCS0 is initialized at reset for boot-ROM selection.
nOE	Output Enable. Low-true output, nOE is asserted during memory reads to enable the data bus drivers of the selected external memory device.
nWE	Write Enable. Low-true output, nWE is asserted during write operations to external memory devices.
RDY	Variable Latency I/O Ready input. Not needed in this design example.

3.0 Interface Considerations

This design example uses two 28F128L18 flash memory devices connected to the Intel® PXA270 processor on a 32-bit wide data bus. It is assumed that the Intel® L18 flash memory is located in the boot space of the Intel® PXA270 processor - on exit from reset, the Intel® PXA270 fetches the first instruction from address 0x000 0000, which corresponds to nCS0.

The bus interface timings shown in this application note are based on a CLK_MEM frequency of 104 MHz, and an SDCLK0 frequency of 52 MHz. Other bus speeds and memory sizes can be substituted by changing the appropriate processor and flash memory register settings described in the following sections.

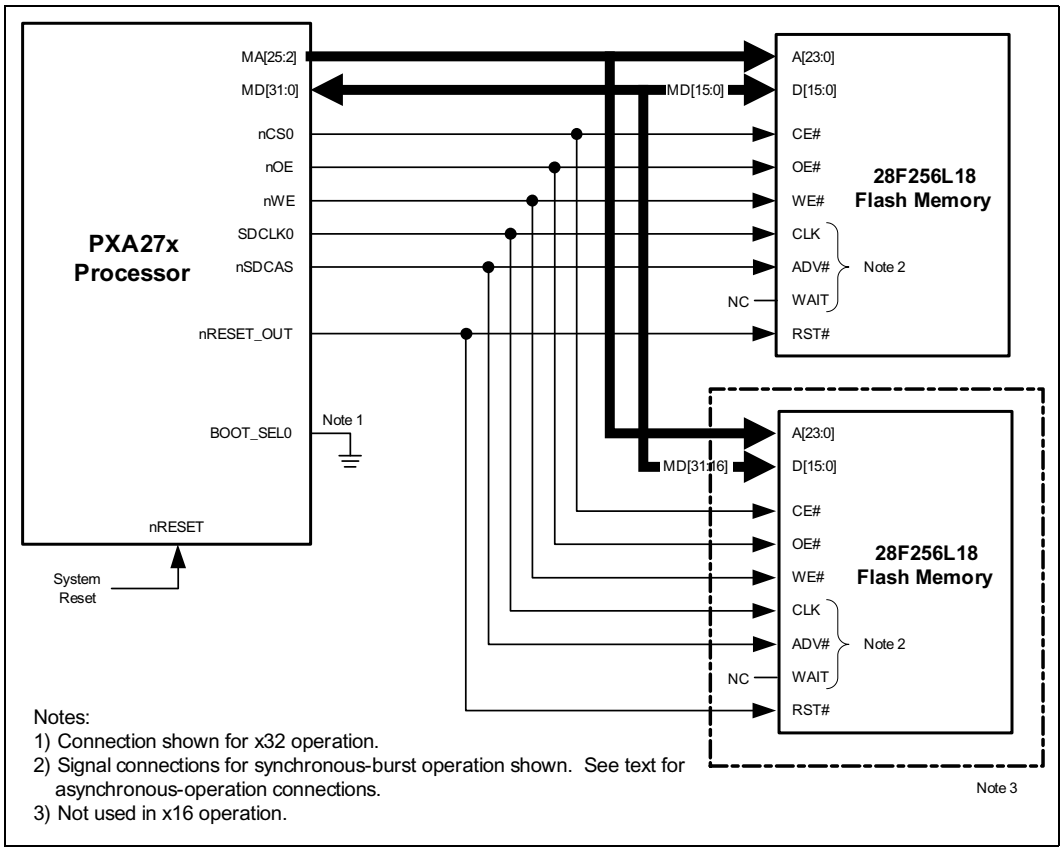
Note: This sample interface design does not include all information regarding system initialization, interrupt control, exception handling, or other peripheral device operations. External device signals/pins should be asserted or deasserted as necessary for desired device operation. Also, proper power supply voltages must be applied in accordance with the latest datasheet information. Be sure to read all applicable documentation (e.g., datasheets, user manuals, specification updates) before attempting this interface.

3.1 Hardware Connections

Figure 2 on page 10 shows the hardware connections between the Intel® L18 flash memory and the Intel® PXA270 processor. This design example uses chip select nCS0, however, any of the other static memory chip selects can be used instead by configuring the appropriate chip select registers. Also, note that only nCS[3:0] support synchronous-burst reads.

At start-up (reset), the Intel® PXA270 processor samples the BOOT_SEL0 input pin to determine the bus width of the boot memory device. In this design example, the two flash memories are arranged in a x32 configuration; therefore, BOOT_SEL0 is shown grounded (low) for a 32-bit boot memory configuration. For a x16 boot configuration, BOOT_SEL0 would be pulled high.

Figure 2. Hardware Connections



A0 on each of the flash memories is the least significant word (x16) address bit. With two devices in a x32 configuration, the least significant double-word (x32) address bit of the Intel® PXA270 processor is A2, and is connected to A0 on each of the flash memories. The rest of the address bits are connected sequentially up to the most significant address bit. Lower-density flash memories can be used as well, in which case, the unused most significant bit (MSB) address bit(s) from the Intel® PXA270 would not be used.

For synchronous-burst read operations, SDCLK0 from the Intel® PXA270 is used for the flash burst clock. However, if only asynchronous read operations are used (including page mode), the CLK input of the flash memories can be tied high and the ADV# input can be tied low.

With nRESET_OUT on Intel® PXA270 connected to the RST# input on the flash memories, a system reset will cause both the Intel® PXA270 and the Intel® L18 flash memory to reset. The flash memories will also reset for "soft" reset events such as Sleep, Watchdog Reset, and GPIO Reset. Refer to the *Intel® PXA27x Processor Family Developer's Manual* for details regarding nRESET_OUT operation.

Note: The Intel® PXA270 nRESET_OUT signal is part of the internally-generated VCC_REG power domain. VCC_REG is switched between VCC_BATT (2.25 V to 3.75 V) and VCC_IO (2.69 V to

3.63 V). Therefore, a suitable voltage-level shifter or voltage-divider network is necessary when connecting nRESET_OUT to RST# of the flash memory.

In all cases, resetting the Intel® L18 flash memory(s) causes them to default to asynchronous read-array mode. If the flash had been previously operating in synchronous-burst mode or a non-array read state (e.g., Read ID, read Status Register, etc.), the appropriate commands must be issued to the flash memories to return them to their previous non-array read state or operating mode.

4.0 Register Settings

On reset, the Intel® PXA270 memory controller registers and the Intel® L18 flash memory Read Configuration Register (RCR) default to their reset values. Refer to the *Intel® PXA27x Processor Family Developer's Manual* and the Intel® L18 flash memory datasheet for the default register settings (see Appendix A, "Additional Information").

During system initialization, the Intel® PXA270 processor and Intel® L18 flash memory registers must be programmed with the appropriate values in order to utilize the synchronous burst-mode read feature of the Intel® L18 flash memory.

Caution: Care must be taken when changing to synchronous mode. Instructions for the RCR configuration sequence must either be in RAM or guaranteed not to fetch from the flash during the RCR programming operation. Access to the flash memory cannot occur until both the Intel® PXA270 and the Intel® L18 flash memory are in synchronous read mode.

4.1 Intel® Flash Memory Register Settings

The default read mode of the Intel® L18 flash memory is asynchronous read array mode, featuring a 4-word page buffer. To enable synchronous burst mode, the Read Configuration Register (RCR) of both flash memories must be programmed. The default value of the RCR is 0xFFFF.

For this example, programming the RCR of each flash device with a value of 0x25C2 configures each flash device for synchronous burst reads as follows:

- Read Mode (RCR.15) = 0b0 (Synchronous Burst Mode)
- RCR.14 = 0b0 (reserved)
- Latency Count (RCR[13:11]) = 0b100 (Code 4)

The latency count is calculated for a 52 MHz burst clock. See the Intel StrataFlash® Wireless Memory (L18) Datasheet.

Note: datasheet for details.

- WAIT Polarity (RCR.10)= 0b1 (default value; not used)
- Data Hold (RCR.9)= 0b0 (hold data for one clock)
- WAIT Delay (RCR.8) = 0b1 (default value; not used)
- Burst Sequence (RCR.7) = 0b1 (linear burst sequence)
- Clock Edge (RCR.6) = 0b1 (rising edge)
- RCR[5:4] = 0b00 (reserved)

- Burst Wrap (RCR.3 = 0b0 (Wrap; accesses wrap within selected burst length)
- Burst Length (RCR[2:0]) = 0b010 (8 words)

This design example uses two flash memory devices arranged in a x32 data bus configuration. Since the Intel® PXA270 has a cache-line fill-buffer size of 256 bits, a burst-of-eight access is used to fetch 256 bits (8 x 32 bits) from the two flash memories. If only one x16 flash memory were used instead, a burst-of-sixteen would be required to fetch 256 bits (16 x 16 bits).

When programming the RCRs of each flash memory, the desired register value is placed on the *address lines,* while the setup command (0x0060 0060) and confirm command (0x0003 0003) is placed on the *data lines*. The hardware address "offset" (Intel® PXA270 A2 connected to A0 of each flash device) must be taken into account by system software when programming the RCR. See Appendix A, "Additional Information" for details.

4.2 Intel® PXA270 Processor Register Settings

The Intel® PXA270 contains registers used to configure the operation of the external memory interface. The settings of the Core Clock Configuration Register (CCCR), SDRAM Refresh Control Register (MDREFR), Synchronous Static Memory Control Register (SXCNFG), and Static Memory Control Register (MSC[2:0]) are described in the following sections.

Note: Only the register bit fields that affect the memory interface operation with Intel® L18 flash memory are discussed; all other bit fields should be programmed as required to ensure proper device operation.

4.2.1 Core Clock Configuration Register (CCCR)

The Intel® PXA270 processor contains a Clocks Manager to manage its multiple clock sources and power reduction functions. The Core Clock Configuration Register (CCCR) is used to set the memory controller clock (CLK_MEM) frequency. For this design example, the Run-Mode to Oscillator Ratio (L) is set to 8 (CCCR:L[4:0] = 0b01000) to produce a CLK_MEM frequency of 104 MHz.

4.2.2 SDRAM Refresh Register (MDREFR)

MDREFR provides frequency control of the SDCLKs. Since the maximum input clock frequency of the Intel® L18 flash memory is 54 MHz, the K0DB2 bit (MDREFR[14]) must be set (1) to configure SDCLK0 to run at one-half the CLK_MEM frequency, or 52 MHz.

Note: Because the K0DB4 bit overrides the K0DB2 bit, ensure that it is cleared (0). Otherwise, SDCLK0 will be running at one-fourth of the CLK_MEM frequency, or 26 MHz.

4.2.3 Asynchronous Static Memory Control Registers (MSC[2:0])

The Asynchronous Static Memory Control Registers (MSC[2:0]) configure the static memory chip selects nCS[5:0] for asynchronous accesses to each of the six static memory banks. Each MSCx register contains two identical configuration fields - one for each of its corresponding chip-selects.

All timing fields in this register are specified in CLK_MEM cycles. If any of the first four (nCS[3:0]) static memory banks are configured for *synchronous* static memory operation via the SXCNFG register, the corresponding half-word of MSC[1:0] is ignored. However, the data-width

field (RBWx) within the affected half-word is still used. Also, for synchronous flash configurations (SXCNFG:SXTPx = 0b10), the MSCx register values are still used for asynchronous flash *write* timings.

When asynchronous page-mode flash is used, the MSCx:RDFx and MSCx:RDNx fields configure the read delay timings for initial-access and subsequent-access delays, respectively. The MSCx:RTx field configures the type of memory used. TheIntel® L18 flash memory supports 4-word asynchronous page-mode reads.

Programming MCS0[15:0] with 0x1282 configures nCS0 for asynchronous page-mode reads as follows:

- RBUFF0 (MSC0[15]) = 0b0 (Slower device - Return Data Buffer)
- RRR0 (MSC0[14:12]) = 0b001 (ROM/SRAM recovery time)
- RDN0 (MSC0[11:8]) = 0b0010 (ROM delay next access)
- RDF0 (MSC0[7:4]) = 0b1000 (ROM delay first access)
- RBW0 (MSC0[3]) = 0b0 (ROM bus width: 32 bits)
- RT0 (MSC0[2:0]) = 0b010 (ROM type: burst-of-four ROM or flash, w/ non-burst writes)

4.2.4 Synchronous Static Memory Configuration Register (SXCNFG)

The external memory interface of the Intel® PXA270 processor supports SDRAM, synchronous burst and asynchronous page mode flash, SRAM, Variable-Latency I/O (VLIO), PCMCIA and Compact Flash expansion memory. Only four of the six static memory banks (nCS[3:0]) can be configured for synchronous-burst flash memory operation. SXCNFG[15:0] configures chip select pair nCS[1:0], while SXCNFG[31:16] configures chip select pair nCS[3:2].

For this design example, programming SXCNFG[15:0] with 0x2011 configures nCS0 (Static Bank 0) for synchronous burst-mode reads with the Intel® L18 flash memory as follows:

- SXCLEXT0 (SXCNFG[15] = 0b0 (CAS latency extension - used w/ SXCL0 for a 4-bit field)
- SXLATCH0 (SXCNFG[14]) = 0b0 (Reserved)
- SXTP0 (SXCNFG[13:12]) = 0b10 (Burst-of-Eight Synchronous Flash)

Note: In this design example, a burst-of-eight access is shown to fetch 256 bits (8 x 32 bits) from the two flash memories for 256-bit cache-line fills. If only one x16 flash memory is used instead, a burst-of-sixteen would be required to fetch 256 bits (16 x 16 bits).

- SXCNFG[11:5] = 0b0000000 (Reserved)
- SXCL0 (SXCNFG[4:2]) = 0b100 (CAS latency of 5 SDCLKs)
- SXEN0 (SXCNFG[1:0]) = 0b01 (Static Bank 0 enabled for SX memory)

5.0 Bus Operation and Timings

For the following discussions, consult the appropriate Intel® PXA270 processor and Intel® L18 flash memory documents for specific timing information of the individual components presented in this design example. See Appendix A, “Additional Information”.

In the following sections, flash memory timings are prefixed with either R (read) or W (write). Since the Intel® PXA270 timings are register dependent, the associated register field names are shown where applicable.

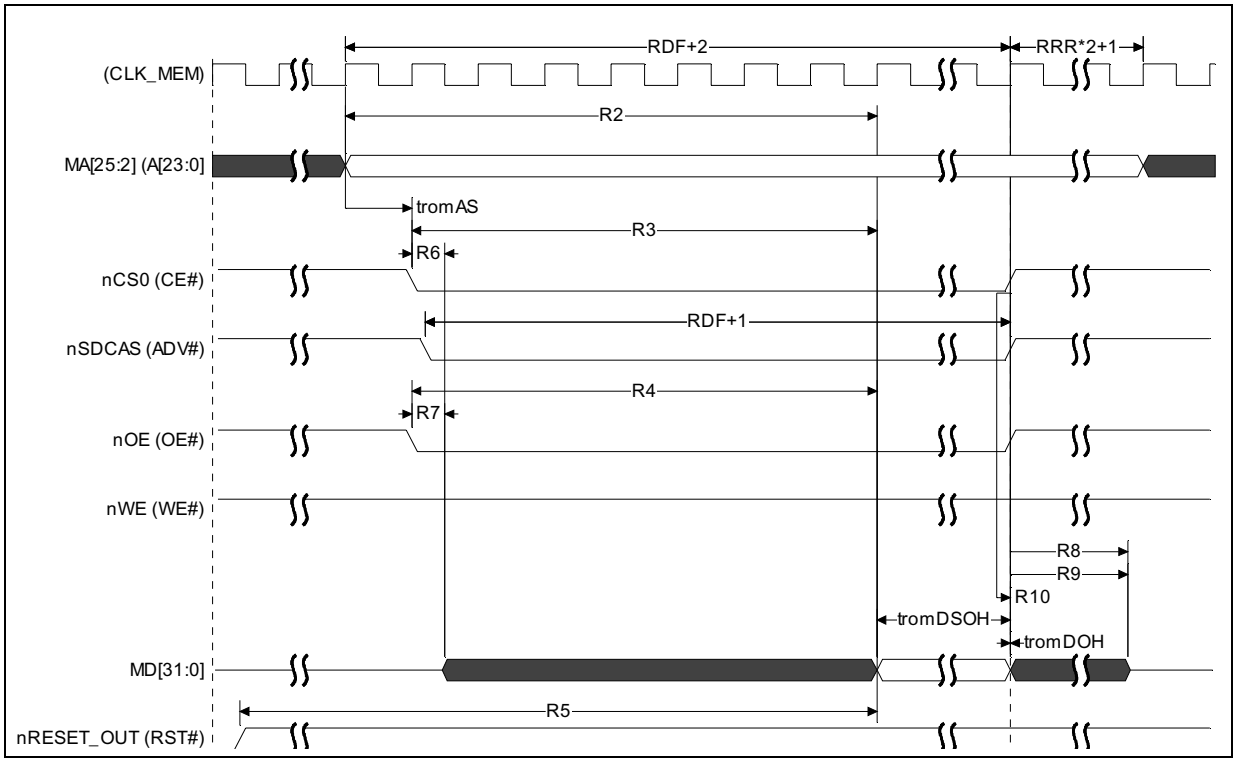
5.1 Asynchronous Single Reads

On power up or reset, the Intel® PXA270 processor memory controller registers default to settings that allow for accessing the slowest ROMs available. In this example, the BOOT_SEL0 pin is tied low (see Figure 2, “Hardware Connections” on page 10) configuring the Intel® PXA270 processor for asynchronous 32-bit ROM with the maximum number of wait states at startup. Similarly, the Intel® 28F256L18 flash memory defaults to asynchronous read-array mode.

Figure 3 shows the bus timings for an initial asynchronous single read following a reset.

Note: R5 must be satisfied before reading from the flash memories.

Figure 3. Asynchronous Single Read



NOTE: CLK_MEM shown for reference only.

5.2 Asynchronous Page-Mode Reads

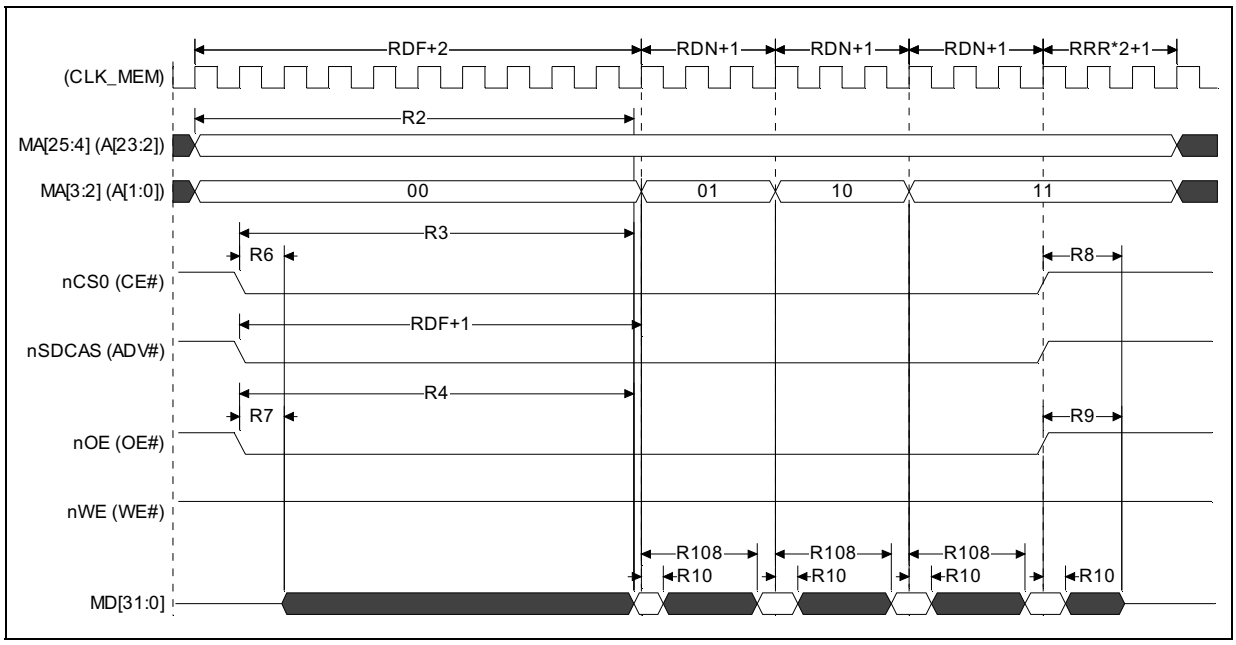
The Intel® 28F256L18 flash memory supports four-word (x16) asynchronous page-mode reads, while the Intel® PXA270 processor supports burst-of-four or burst-of-eight asynchronous read accesses. In this design example using two Intel® 28F256L18 devices on a x32 bus, four double-words (x32) are output using 4-word asynchronous-page mode.

On reset, the Intel® L18 flash memory defaults to array reads in asynchronous page-mode. When a read occurs, four words are sensed from the flash array and copied into a high-speed page buffer, with the addressed word being output after all initial access delays (tAVQV, tELQV, and tGLQV) have been satisfied.

The low-order memory addresses A[1:0] of the flash memories are driven by the processor's lower two non-byte addresses (MA[3:2]) to access x32 data from the two flash devices' page buffers; no flash commands are necessary for asynchronous page-mode operation.

Figure 4 shows the bus timings for burst-of-four, asynchronous page-mode array reads.

Figure 4. Asynchronous Page-Mode Reads



NOTE: CLK_MEM is shown for reference only.

5.3 Synchronous Burst-Mode Reads

The Intel® L18 flash memory supports 4-, 8-, 16-, and continuous-word synchronous burst reads, whereas, the Intel® PXA270 processor supports 8- and 16-word synchronous-burst reads. Since the cache-line fill buffer on Intel® PXA270 is 256 bits and the bus width in this design example is 32 bits, 8-word burst is used (32 bits x 8 = 256 bits).

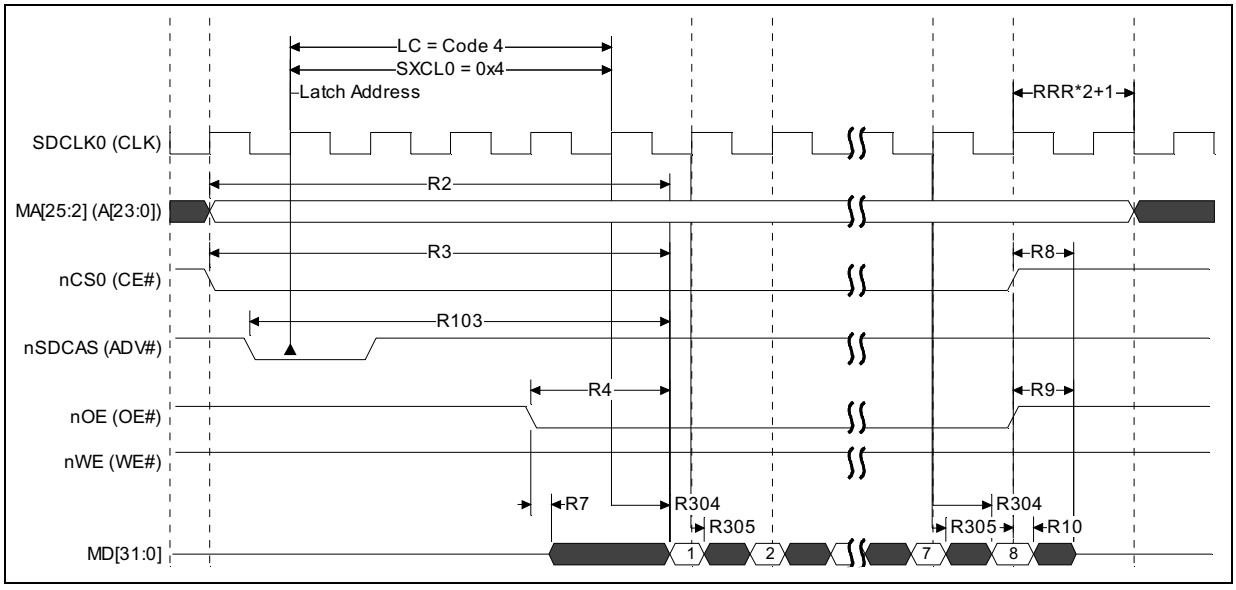
At the start of a synchronous-burst read cycle, the Intel® PXA270 processor drives a valid address onto MA[25:2]. One CLK_MEM cycle later, nCS0 and nSDCAS are asserted. The next rising edge of SDCLK (CLK) with nSDCAS (ADV#) low signals the flash memories to latch the initial burst address. nSDCAS remains low for three CLK_MEM periods, then deasserts.

OE# asserts two SDCLK cycles before valid data is sampled. For this design example with a CAS latency code of 4, OE# asserts two SDCLK cycles after nSDCAS deasserts.

After the initial-access latency period has elapsed, the Intel® PXA270 processor samples the read data on the rising edge of SDCLK. Subsequent burst reads are sampled on the rising edge of SDCLK with zero wait states.

Figure 5 shows the timing for a burst-of-eight, x32 synchronous-read bus access.

Figure 5. Synchronous Burst-Mode Reads



5.4 Asynchronous Writes

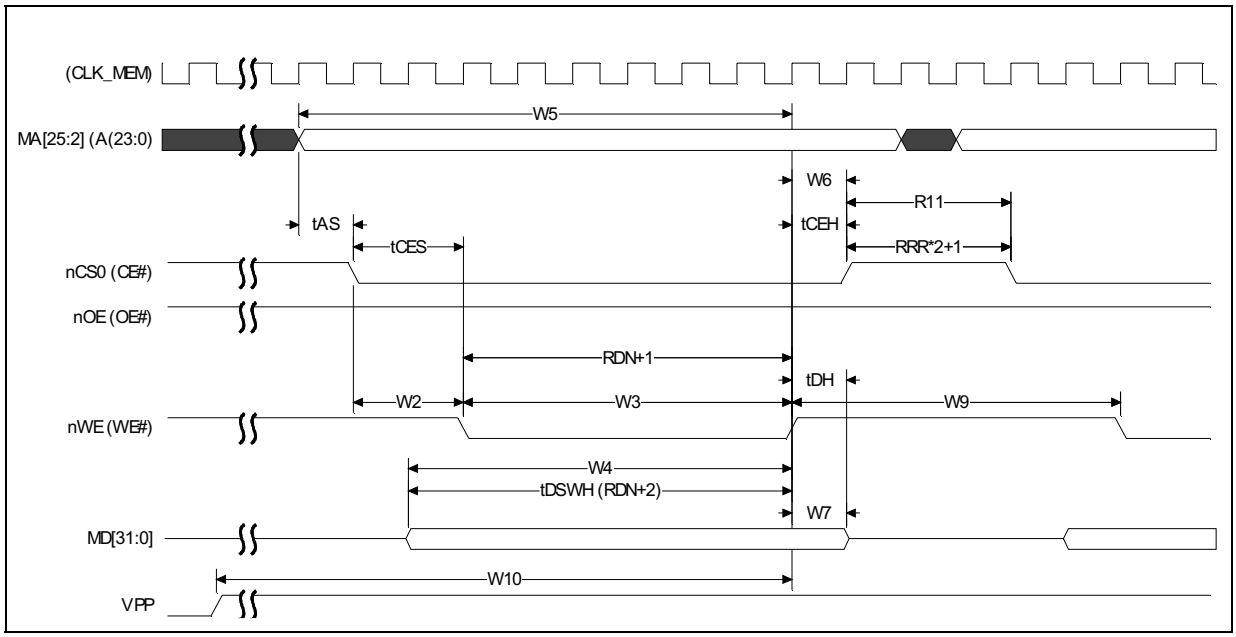
The value programmed into MSC0:RDN0 determines the number of CLK_MEM cycles from address to data valid for subsequent reads from page-mode flash or ROM. RDN0 also determines the number of CLK_MEM cycles that nWE (WE#) is asserted for write accesses to flash.

In order to satisfy the flash devices' WE#-low specification (W3), MSC0:RDN0 must be programmed with 0b0101. This will cause nWE (WE#) to assert for six CLK_MEM cycles during write accesses, satisfying W3.

The flash devices sample the write address and write data on the rising edge of nWE (WE#) or nCS0 (CE#), which ever comes first. Write address/ data setup and hold times are satisfied by tDSWH and tDH, respectively.

Figure 6 shows the bus timings for an asynchronous write.

Figure 6. Asynchronous Writes



NOTE: CLK_MEM shown for reference only.

6.0 Summary

Intel StrataFlash® Wireless Memory (L18) utilizes proven and reliable two-bit-per-cell technology, manufactured on 0.13 um lithography. The synchronous burst-mode read feature provides high data transfer rates for memory sub-systems while providing support for different I/O voltages through the use of a separate I/O voltage supply pin.

The flexible interface of Intel StrataFlash® wireless memory provides the system designer with a simple, and sometimes "glueless", interface. This can reduce power consumption, decrease material costs, and increase overall system reliability by eliminating the need for additional interface components.

Intel StrataFlash® wireless memory is available in several densities for system design flexibility, and its VFBGA package is ideal for space-constrained applications. Intel StrataFlash® wireless memory is an excellent option for both code execution and data storage applications where high density and low cost is required.

Appendix A Additional Information

Order Number	Document
251902	Intel StrataFlash® Wireless Memory (L18) Datasheet
292286	AP-738 Reduce Manufacturing Costs with Intel® Flash Memory Enhanced Factory Programming
253856	AP-786 Concurrent Program and Erase Using Intel StrataFlash® Wireless Memory System (LV18/LV30)
280000	Intel® PXA27x Processor Family Developer's Manual
280002	Intel® PXA270 Processor Family Electrical, Mechanical, and Thermal Specification
280014	Interfacing to the Intel®PXA27x Processor Family Application Note

NOTES:
1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit the Intel home page at http://www.Intel.com for technical documentation and tools.
3. For the most current information on Intel flash products, visit http://developer.intel.com/design/flash