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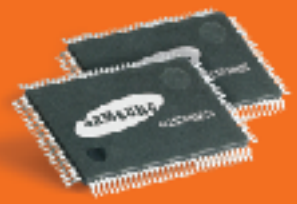
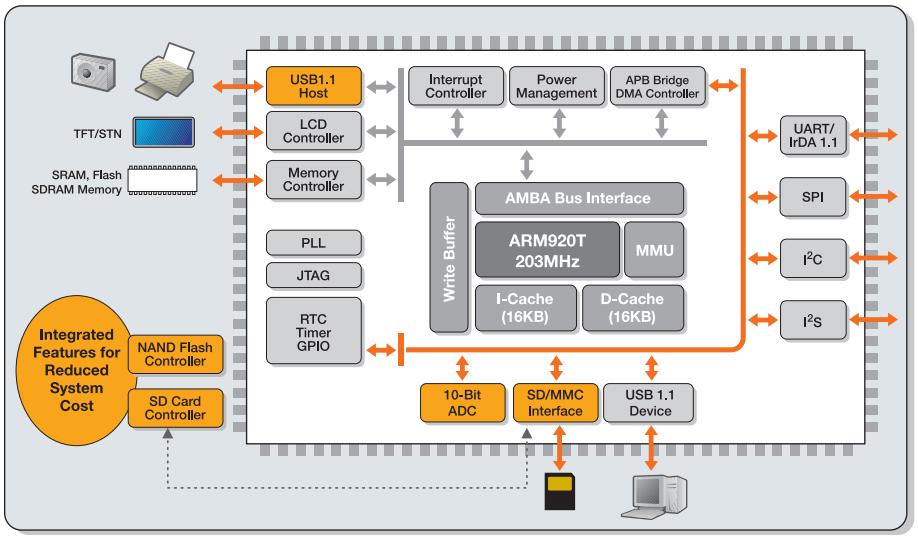


Samsung S3C2410

World's First ARM-Based Processor with NAND Flash Support

Design Innovation for Mobile Computing

Samsung's S3C2410 16/32-bit RISC microprocessor is designed to provide a cost effective, low power, small die size and high performance microcontroller solution for hand held devices and general mobile applications. To reduce total system cost, the S3C2410 also provides the following features: separate 16KB Instruction and 16KB Data Cache, MMU to handle virtual memory management, LCD controller (STN & TFT), NAND flash bootloader, System Manager (chip select logic, SDRAM controller), 3 channel UART with handshake, 4 channel DMA, 4 channel Timers with PWM, I/O Ports, RTC, 8-channel 10-bit ADC and a touch screen interface, I2C-BUS interface, I2S-BUS interface, USB Host, USB Device, SD Host and Multimedia Card Interface, 2-channel SPI and PLL for clock generation.



- *By providing a complete set of common system peripherals, the S3C2410 minimizes overall system costs and eliminates the need to configure additional components.*

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The S3C2410 is developed using an ARM920T core, 0.18um CMOS standard cells and a memory compiler. Its low power, simple, elegant and fully static design is particularly suitable for cost and power sensitive applications. Also, the S3C2410 adopts a new bus architecture, AMBA (Advanced Microcontroller Bus Architecture). An outstanding feature of the S3C2410 is its CPU core, a 16/32-bit ARM920T RISC processor designed by Advanced RISC Machines, Ltd. By providing a complete set of common system peripherals, the S3C2410 minimizes overall system costs and eliminates the need to configure additional components.

Features

ARM920T CPU Core

- 64-way set-associative cache with: I-Cache (16KB) and D-Cache (16KB)
- Write-through and Write-back cache operation
- MMU supports MS WinCE, LINUX, Palm OS and Symbian
- Internal AMBA bus architecture

System Manager

- Little/Big-Endian support
- Address space: Total 1Gbyte
- NOR/Strata flash, ROM, SRAM, and SDRAM
- NAND flash bootloading

Operating Conditions

- Internal: 1.8V/2.0V
- External I/O: 3.3V
- The Maximum: 203MHz@1.8V 266MHz@2.0V
- 2.5V/3.3V memory interface

Package

- 272 FPBGA (14 Body)

Benefits

- Built-in NAND flash bootloader, SD Host
- Various Embedded IP
- Design Time Reduction with a Supporting Reference Board & RTOS
- Various Design Applications

Key Applications

- Smartphone
- Wireless PDA
- 3G Phone
- Telematics
- Game Machines

On-Chip Peripherals

- Power Management: Normal, Idle, Slow, Power-off
- 4-channel 16-bit PWM (Pulse Width Modulation), 1-ch 16-bit timer for OS
- RTC: 32.768 KHz, alarm interrupt
- GPIO:117 (multiplexed I/O)
- 3-channel UART
- 4-channel 16-bit DMA controllers
- 8-channel 10-bit A/D (Max. 500KSPS), including TSP controller
- TFT LCD/STN LCD controller (16bit, 640x480 maximum)
- 16-bit watch-dog timer
- 1-channel I2C-bus interface
- I2S-bus interface
- Screen size: up to 640 x 480
- 2-channel SPI (Synchronous Serial I/O)
- SD Host/MMC (Multi Media Card) I/F
- USB host/device interface
  2-channel USB Host Interfaces (1-channel dedicated host and 1-channel selective host/device)
  1-channel USB Device Interface (12Mbps)
- Debug TEST
- NAND Flash controller (4kb internal buffer)
- 24-Channel external interrupts controller (wake-up source 16-Channel)

Samsung's S3C2410 16/32-bit RISC microprocessor is designed to provide a cost-effective, low power, small die size and high performance micro-controller solution for hand-held devices and general mobile applications.

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